# 2009 MURI Review
# A 21st Century Approach to Reliability

## Degradation Studies of 0.15 μm Gate Length InAlAs/InGaAs pHEMT

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# Outline

- Introduction
- Identification of Possible Degradation Mechanisms
- Reliability improvement of Pt/Ti/Pt/Au Gate Metallization
- Ohmic Contact Reliability Improvement
- Conclusion

# Introduction

- In the literature, degradation mechanisms of InAlAs/InGaAs pHEMTs vary from company to company:
  - Ohmic Contact
  - Layer Structure
  - Fluorine Contamination
  - Bias Dependence
  - Gate Recess Depth
  - Gate Metal Sinking
- It is important to identify the degradation origins on its own process techniques to improve the reliability performance

Private communications indicate that ALL InAlAs/InGaAs HEMTs suffer from an initial decrease in $I_{DSS}$ - this is accommodated by a burn-in to get the devices to a new equilibrium.

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# HEMT Reliability (both InP and GaAs)

- What is the cause of the initial degradation-is it related to the usual mechanisms in HEMTs? :
- Contact problems (esp. sinking gates but also Ohmic spiking)
- Surface states (gate lag)
- Hot carrier-induced (impact ionization at gate edge)
- Mechanical stress (H→Ti compressive stress due to piezo effects in InP, del Alamo 1999)
- Corrosion (fig from Meneghesso and Zanoni,Micro.Rel.42,685 (2002)
- F contamination compensating donors in channel

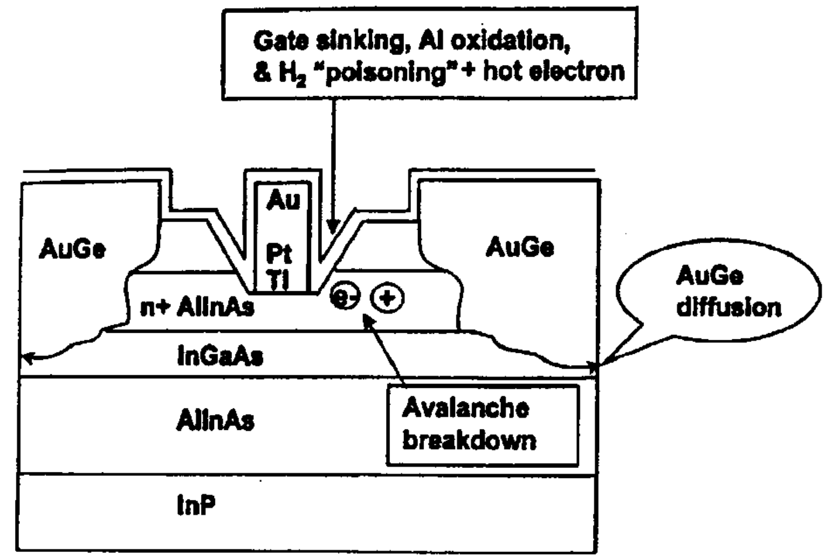


Fig. 1. Schematic cross-section of an InP-based HEMT, identifying the location of possible failure mechanisms.

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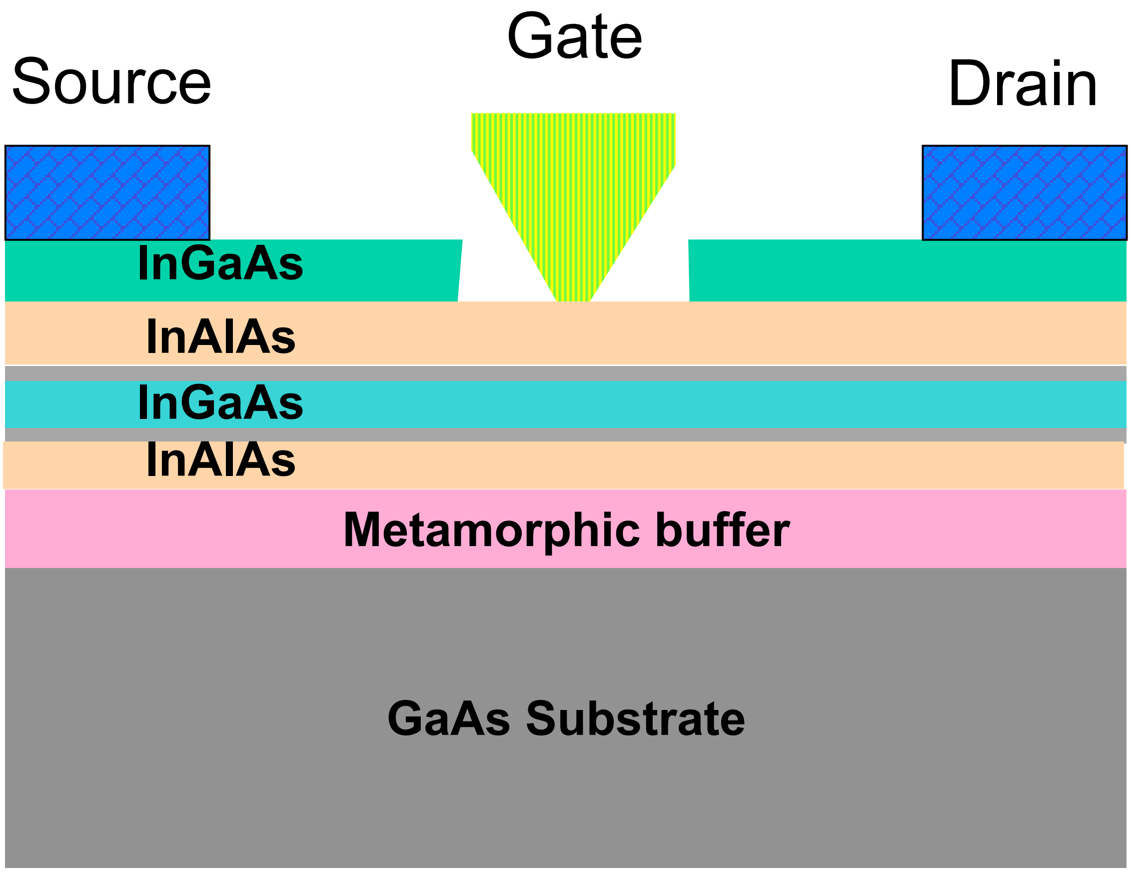
# 0.15 µm Gate Length PHEMT Technology




95 GHz ft process
0.15 µm T-gate
Gm peak 550 mS/mm
IDSS 260 or 500 mA/mm
Vto –0.7 or –1.2V
Slective gate recess
Air Bridge or slot via
Two layer Au interconnect
2 or 4 mil final wafer thickness

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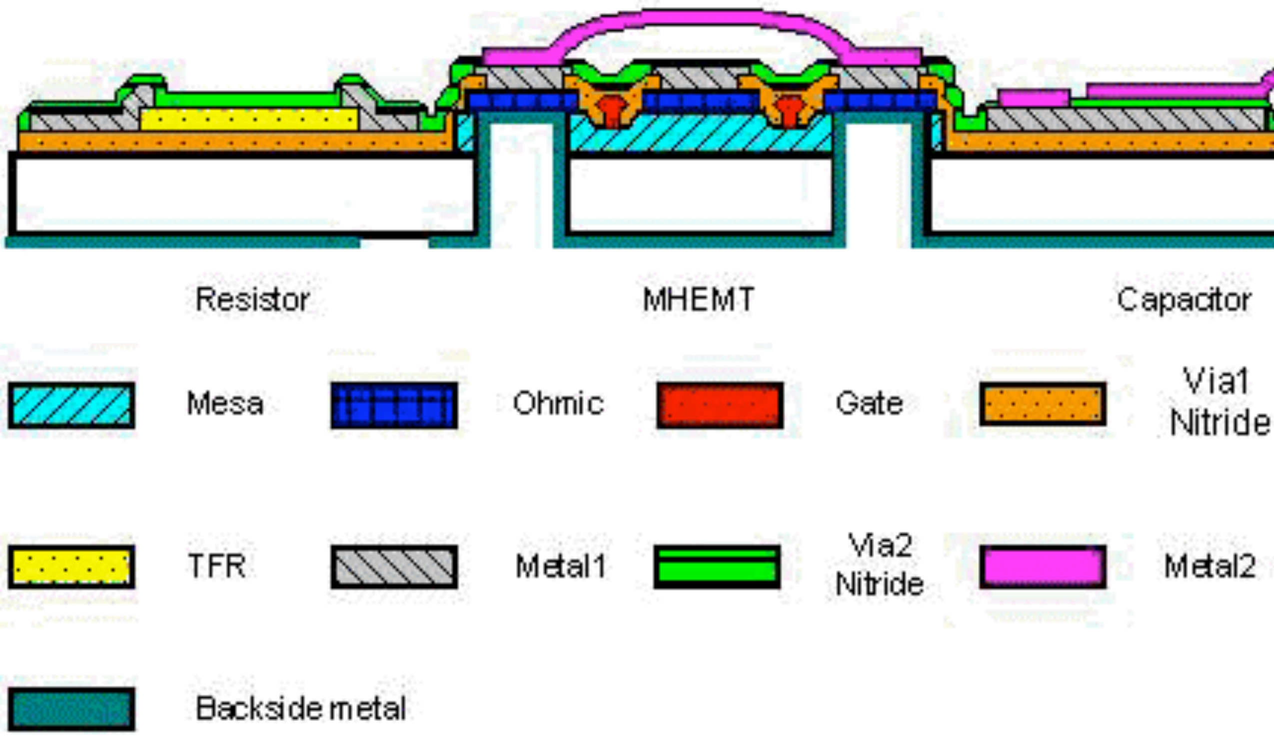
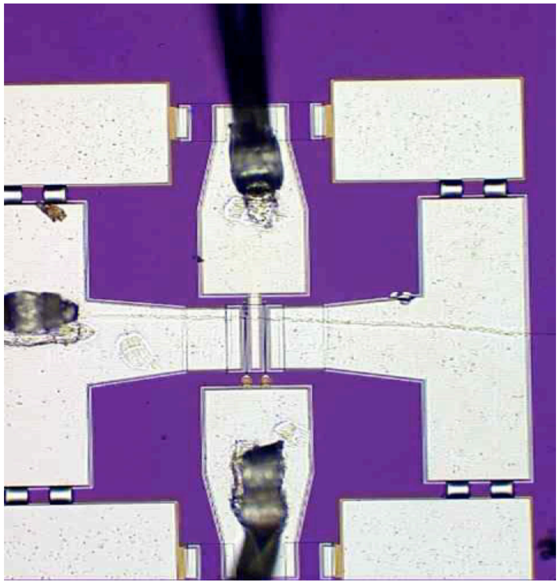
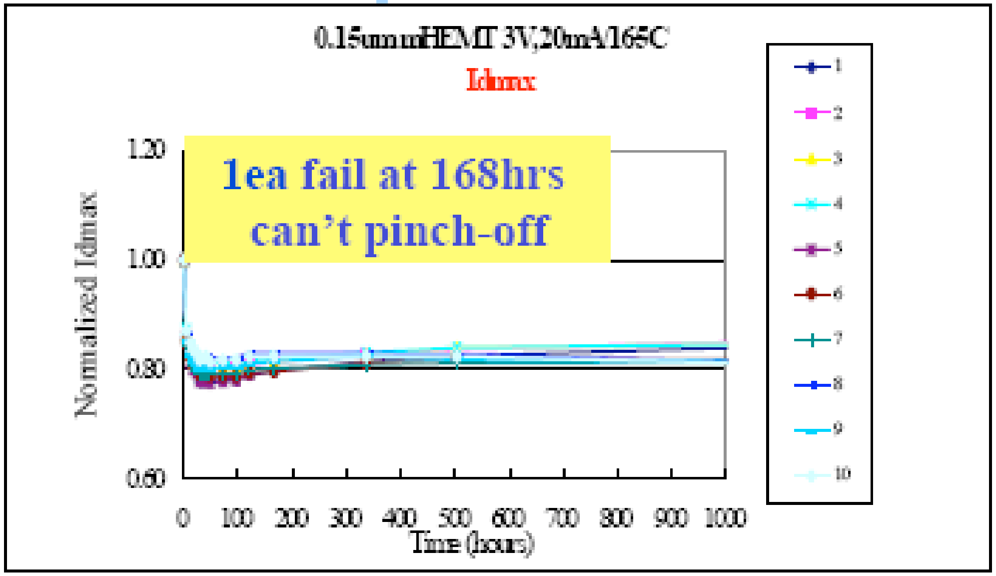
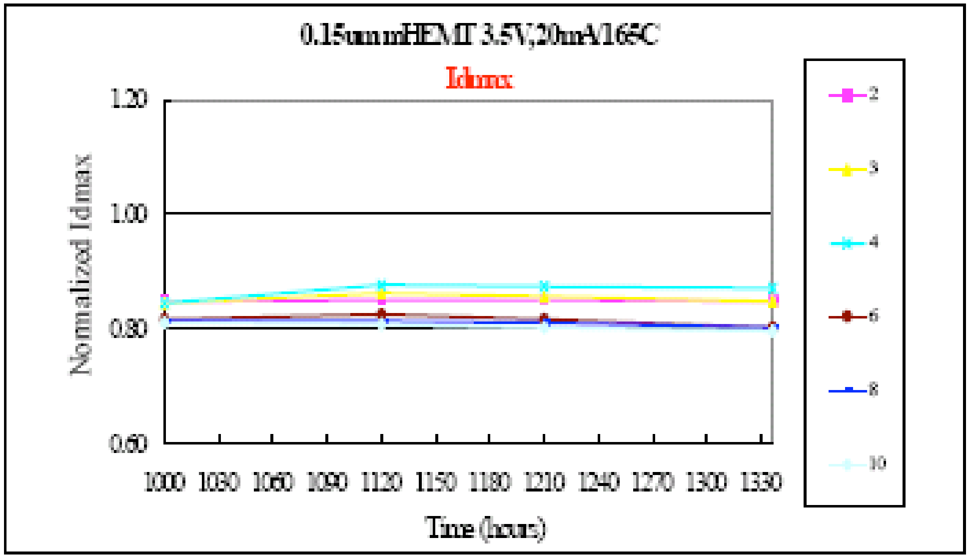
# Schematic of Test Device



# Is it possible to eliminate or reduce the time for burn-in process?

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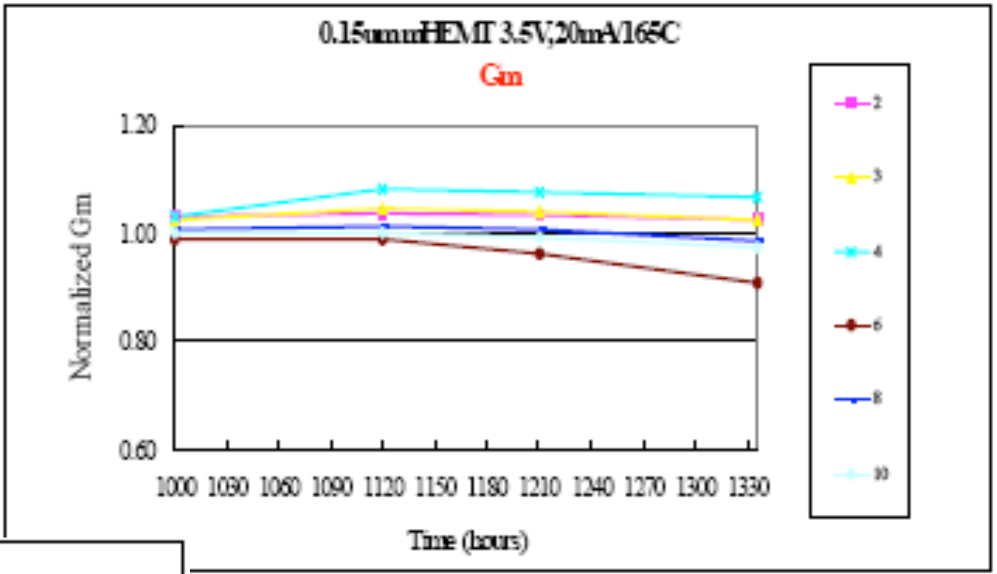
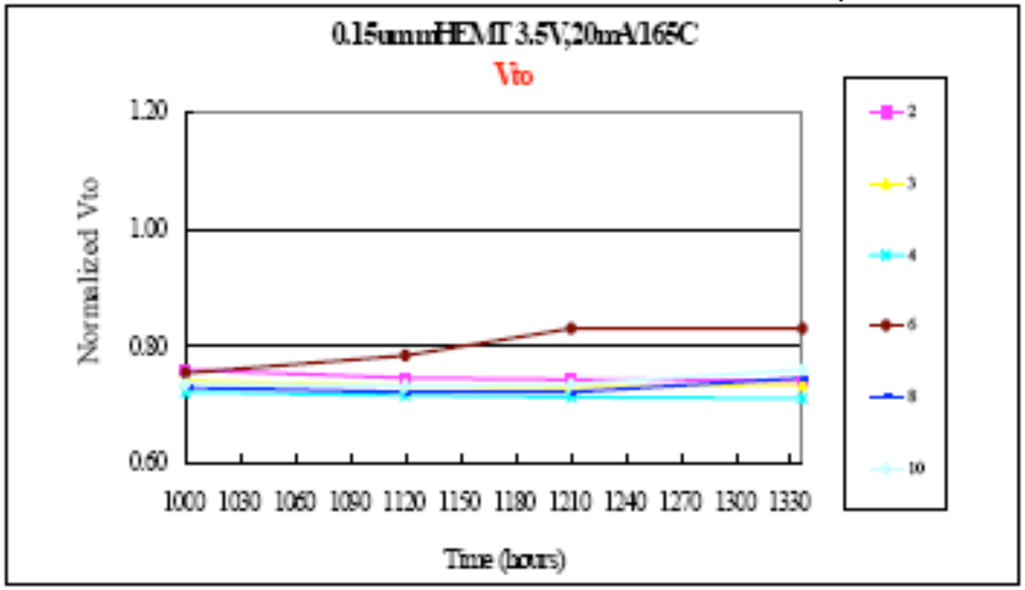
# Extrinsic Transconductance and Threshold voltage

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## Summary of the Stress Test Results

| Time | 0 h | 36 h | 42 h | 48 h |
|---|---|---|---|---|
| Normalized Idmax | 1.0 | 0.86 | 0.85 | 0.84 |
| Normalized Gm-max | 1.0 | 0.97 | 0.96 | 0.96 |
| Normalized Ron | 1.0 | 1.4 | 1.4 | 1.4 |
| Normalized Vto | 1.0 | 0.77 | 0.77 | 0.77 |

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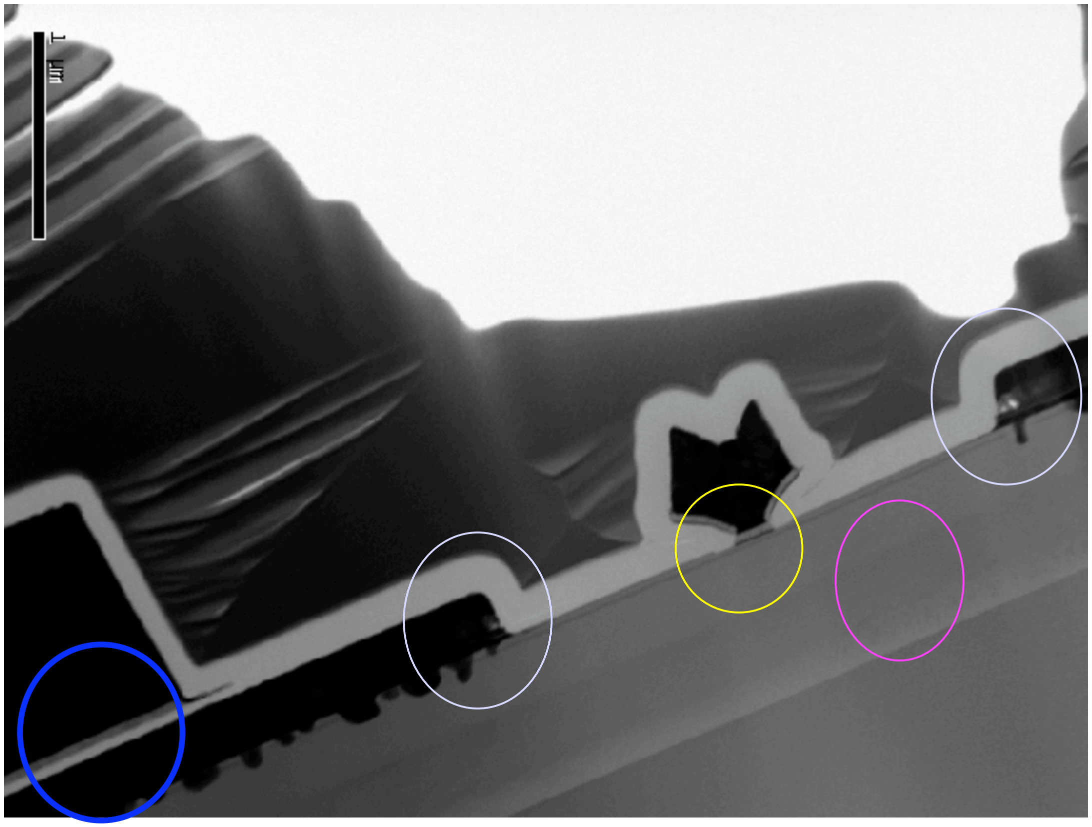
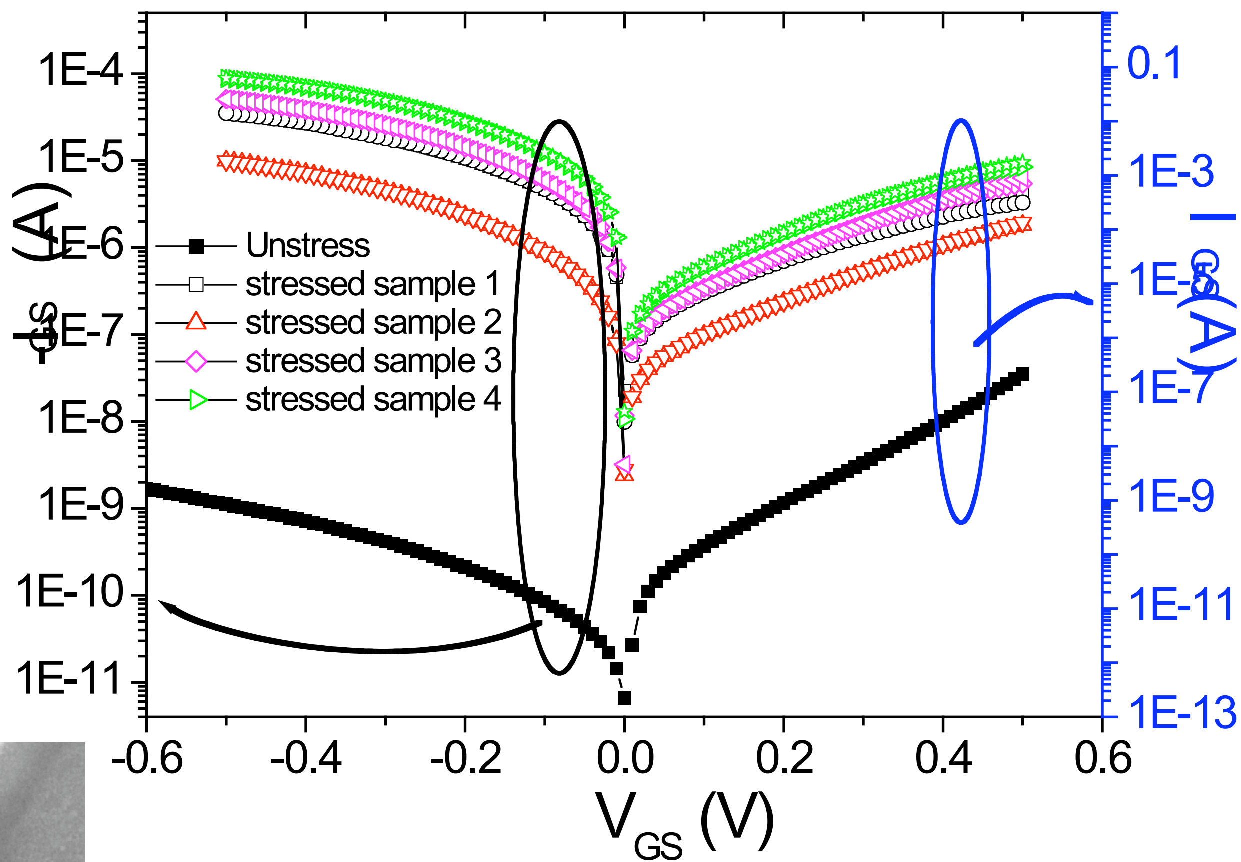
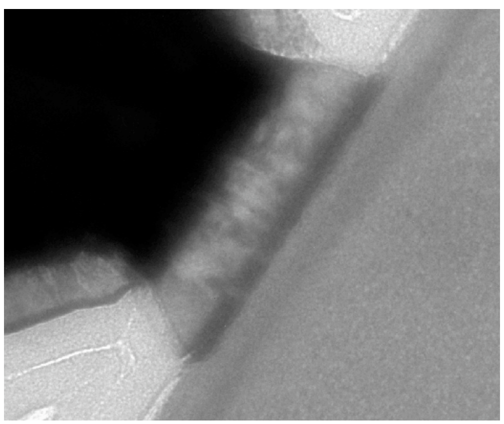
# TEM of Stressed Sample

- Gate Metal Sinking
- Layer Structure
- Ohmic Contact
- Metal Interconnection



# Possible Gate Sinking



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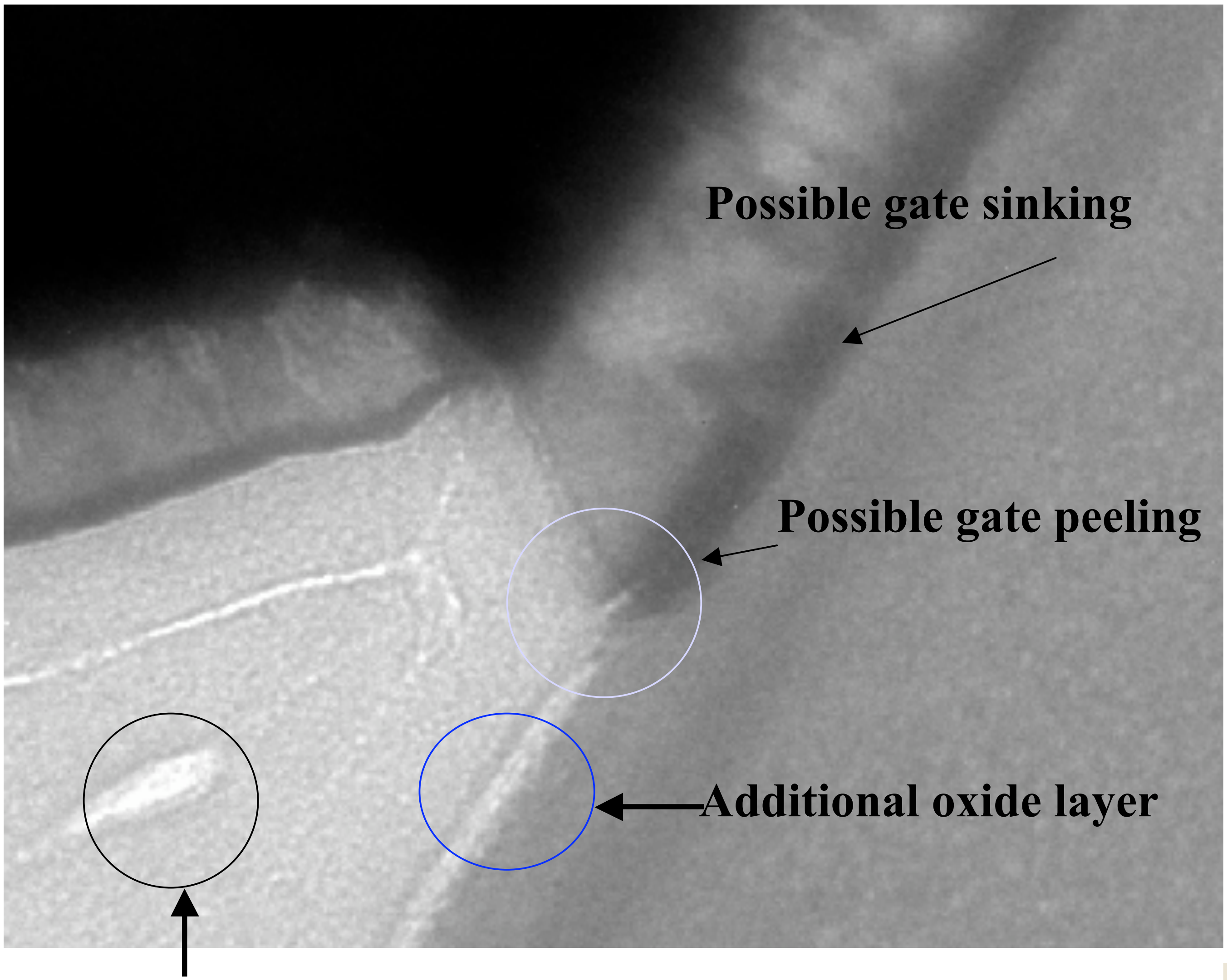
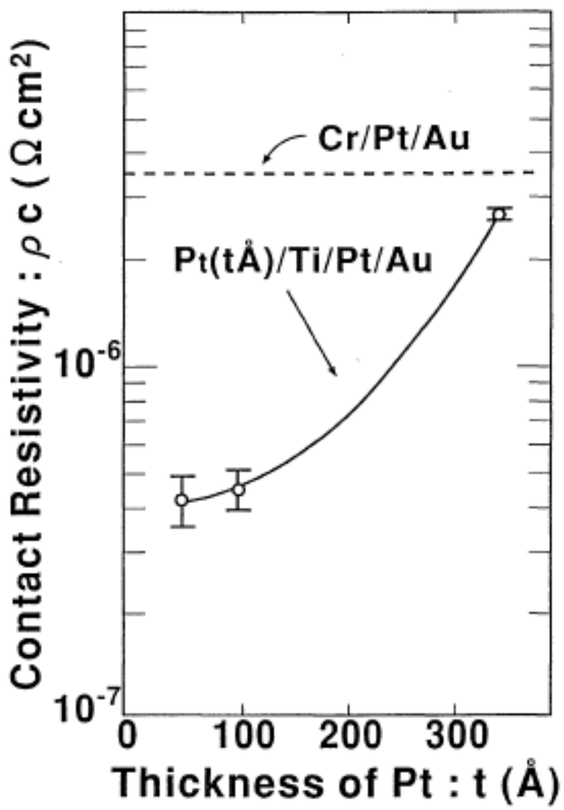
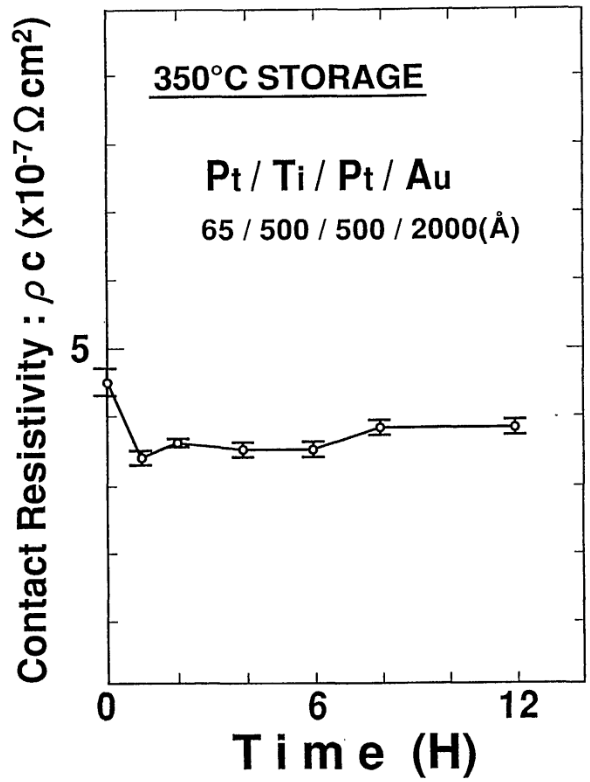
# Possible Gate Sinking



# Pt/Ti/Pt/Au Gate Metal Stack

Pt/Ti/Pt/Au metallization has been used as base contact metal for AlGaAs/GaAs HBT and gate metal for InAlAs/InGaAs HEMT





T. Sugiyama, Jpn. J. Appl. Phys. 33, 786-789, 1994.
S. Hongo, Jpn. J. Appl. Phys. 34, 1181-1184, 1995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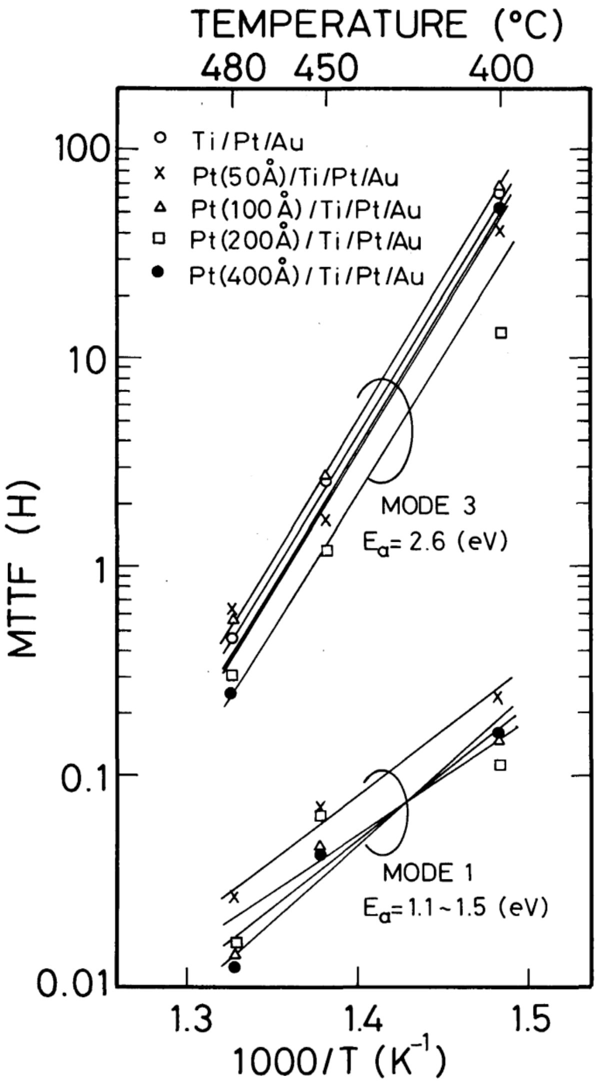
# Reliability of Pt/Ti/Pt/Au used as Ohmic Metallization




H. Okada, Jpn. J. Appl. Phys. 30, L558-L560, 1991

| Interface- Pt Thickness (Å) | $\mu_{50}$ (150 °C) (hour) |
|---|---|
| 50 | $1.2 \times 10^{12}$ |
| 100 | $5.2 \times 10^{11}$ |
| 200 | $3.0 \times 10^{4}$ |
| 400 | $4.2 \times 10^{4}$ |

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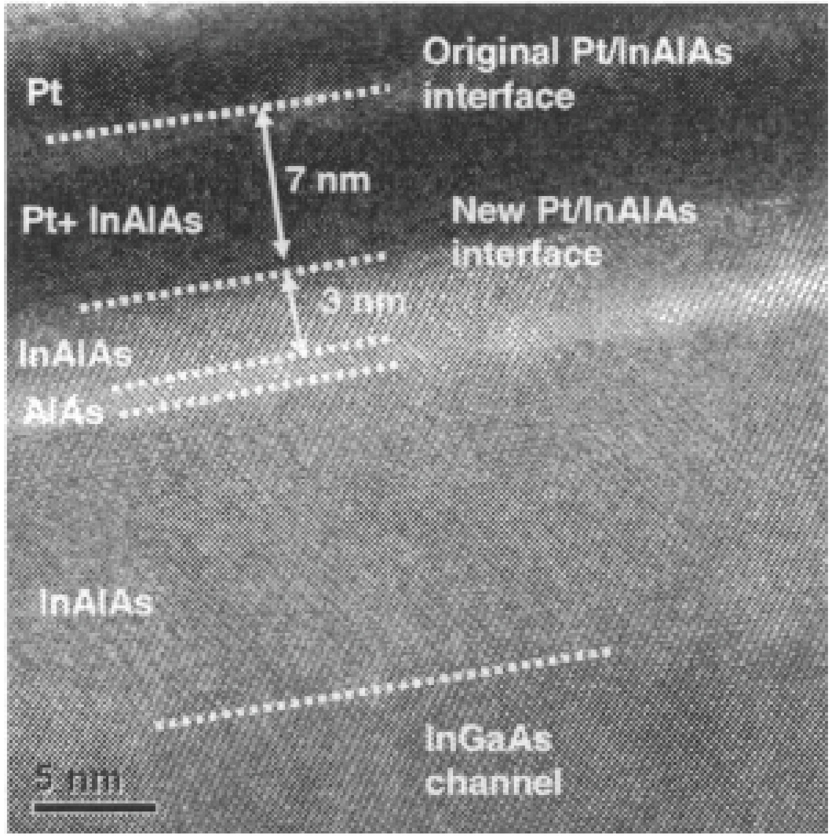
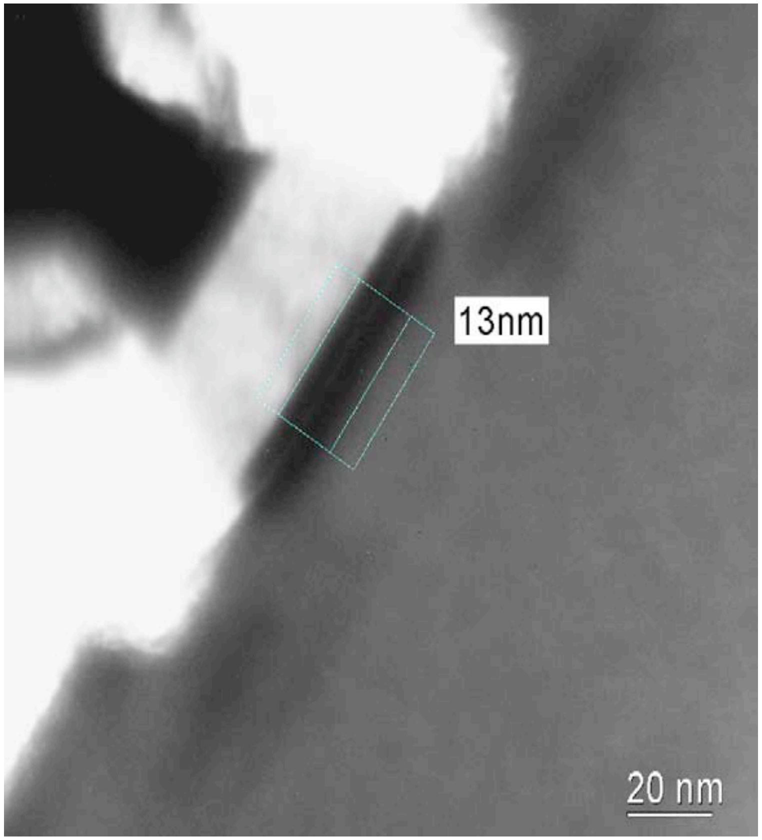
# Pt/Ti/Pt/Au Metallization used as Gate Contact for InAlAs/InGaAs HEMT




I. Adesida, Electron Lett. 41, 2005
I. Adesida, IEDM Abstract 259-260, 2005
M. Dammann, Microelectron. Relia. 44, 934-943, 2004

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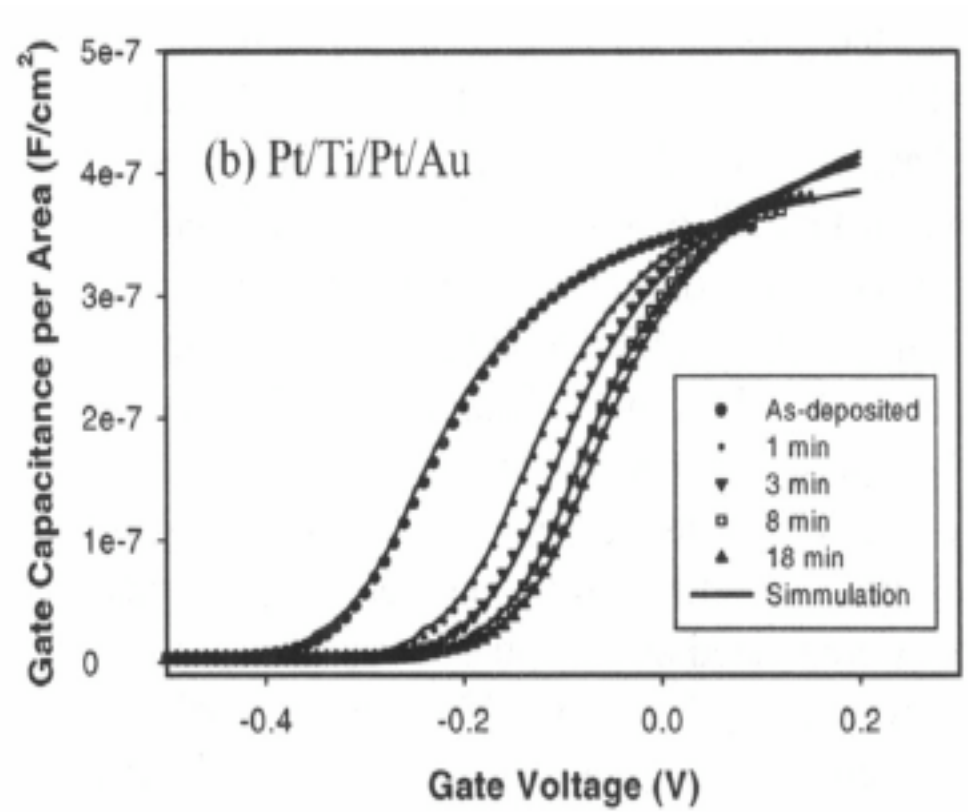
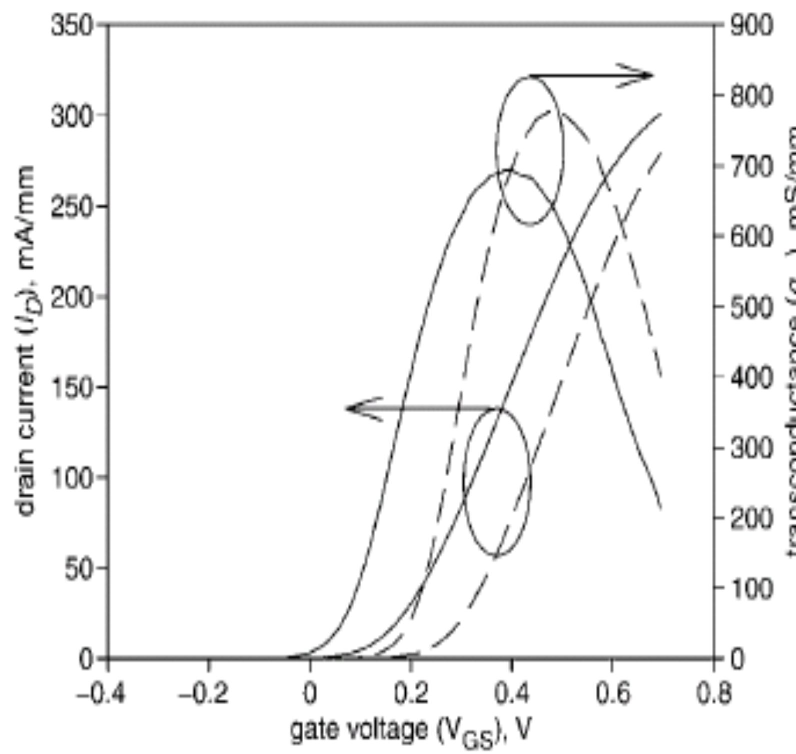
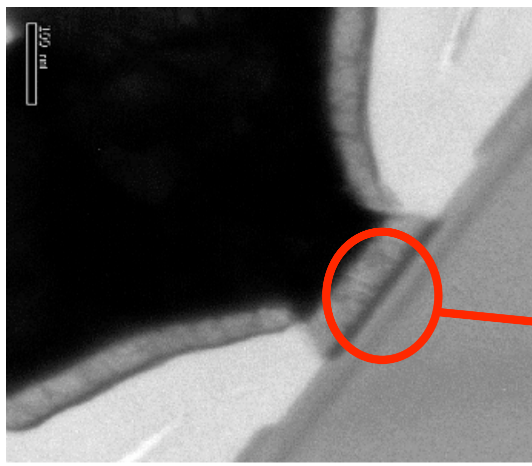
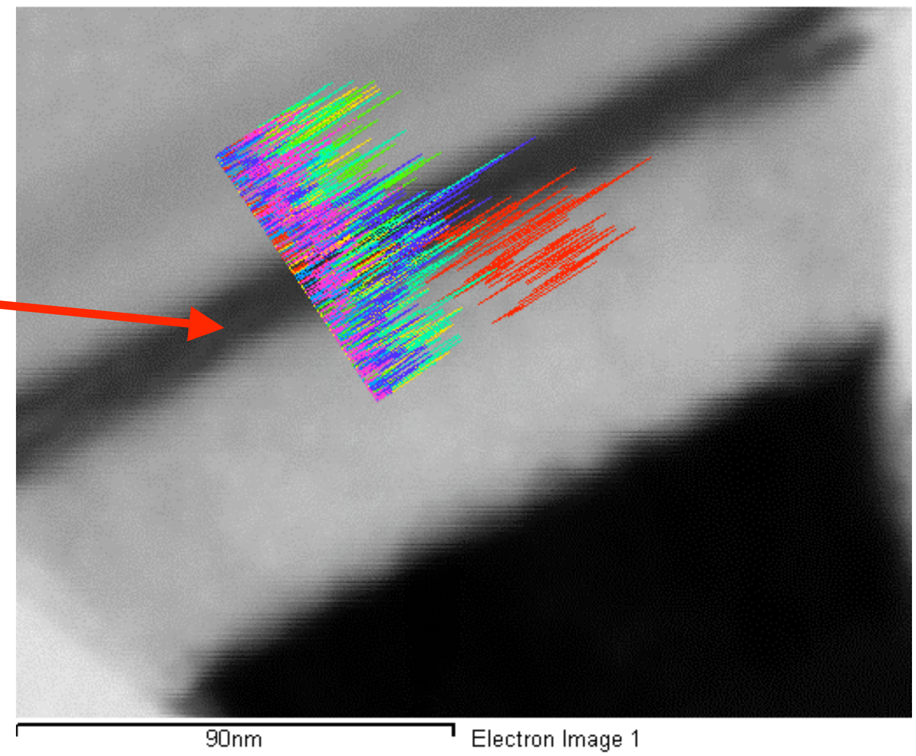
# Pt/Ti/Pt/Au Metallization Used As Gate Contact for InAlAs/InGaAs HEMT

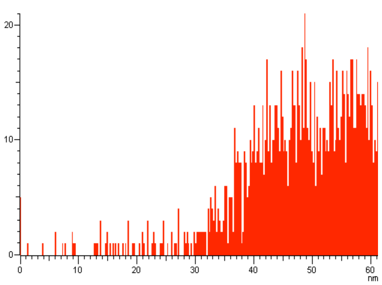


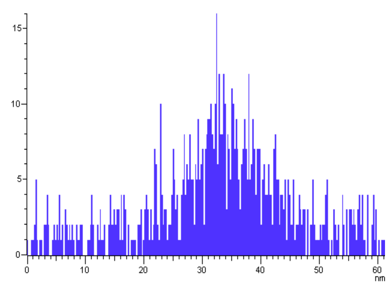

$G_m \propto 1/d_{\text{eff InAlAs layer thickness}}$



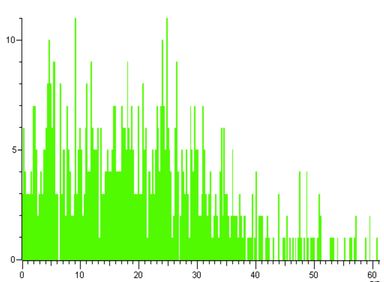


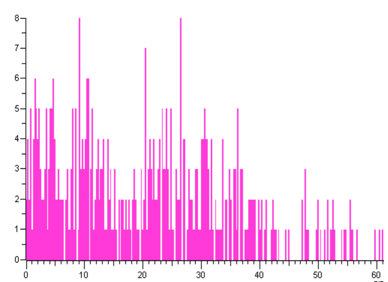
Titanium Ka1



Platinum La1



Arsenic Ka1



Indium La1

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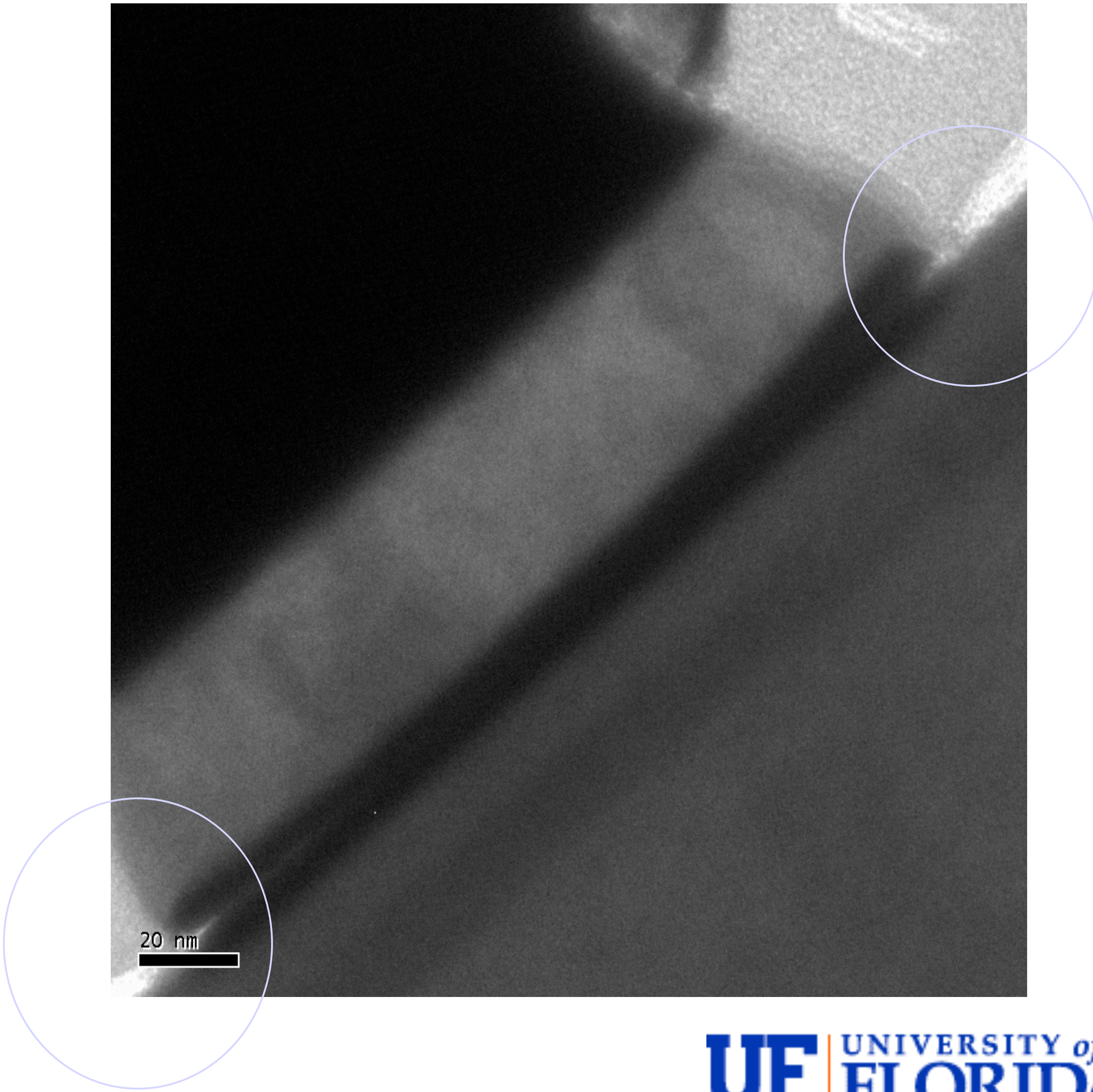
# Possible gate peeling on the UF stressed device

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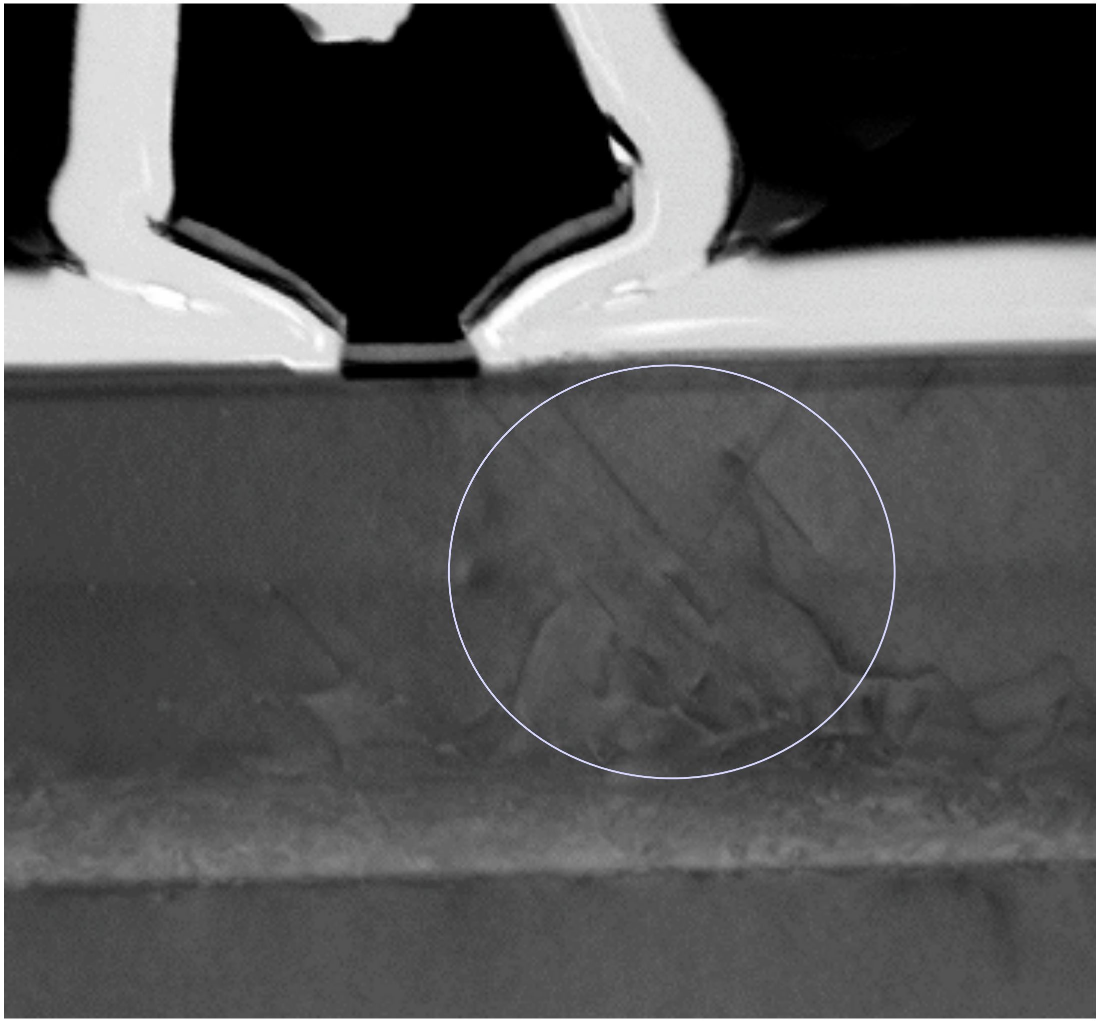
# Dislocations found in the UF stressed device



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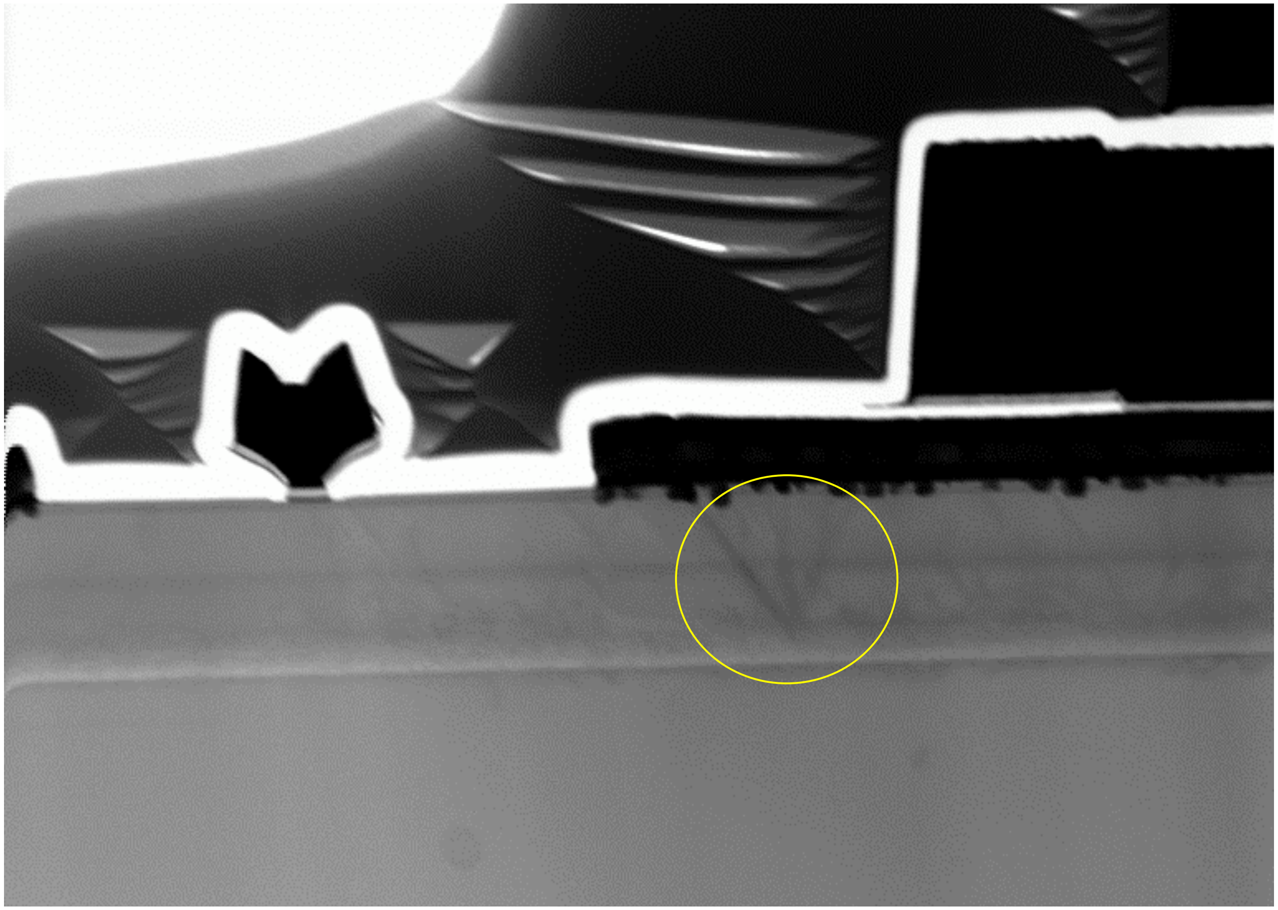
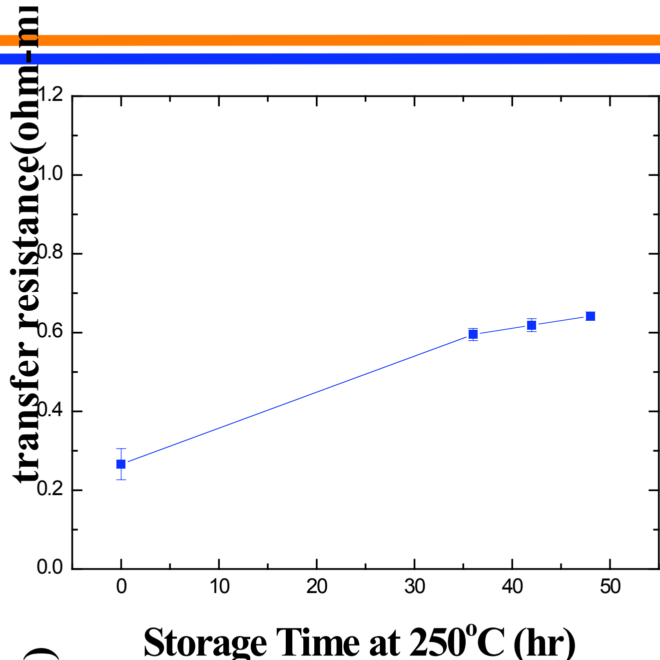
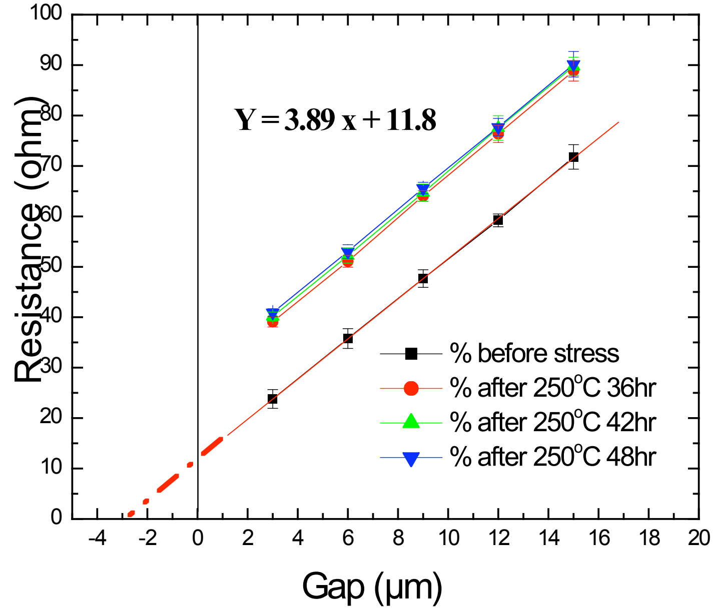
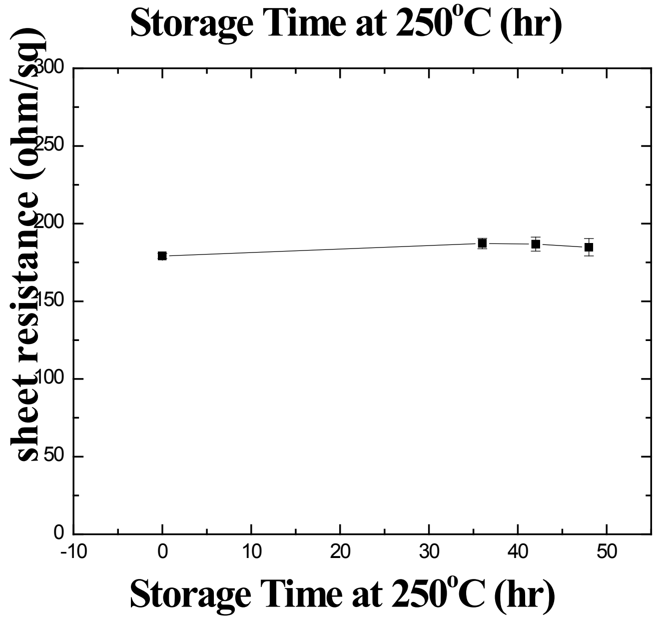
# Dislocations also found in the unstressed device

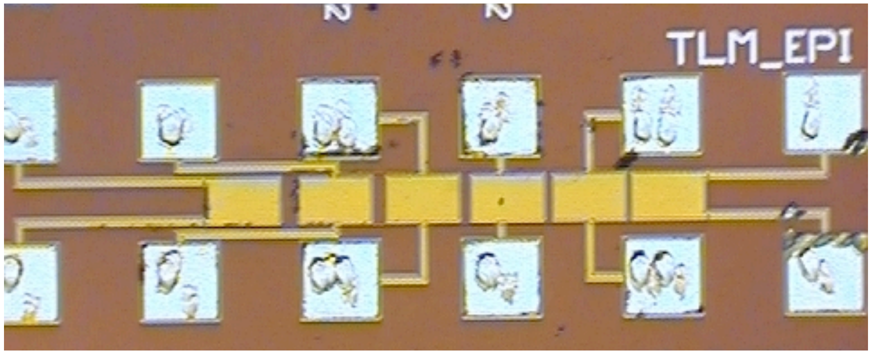


# Current Stress on TLM pattern to isolate gate effect

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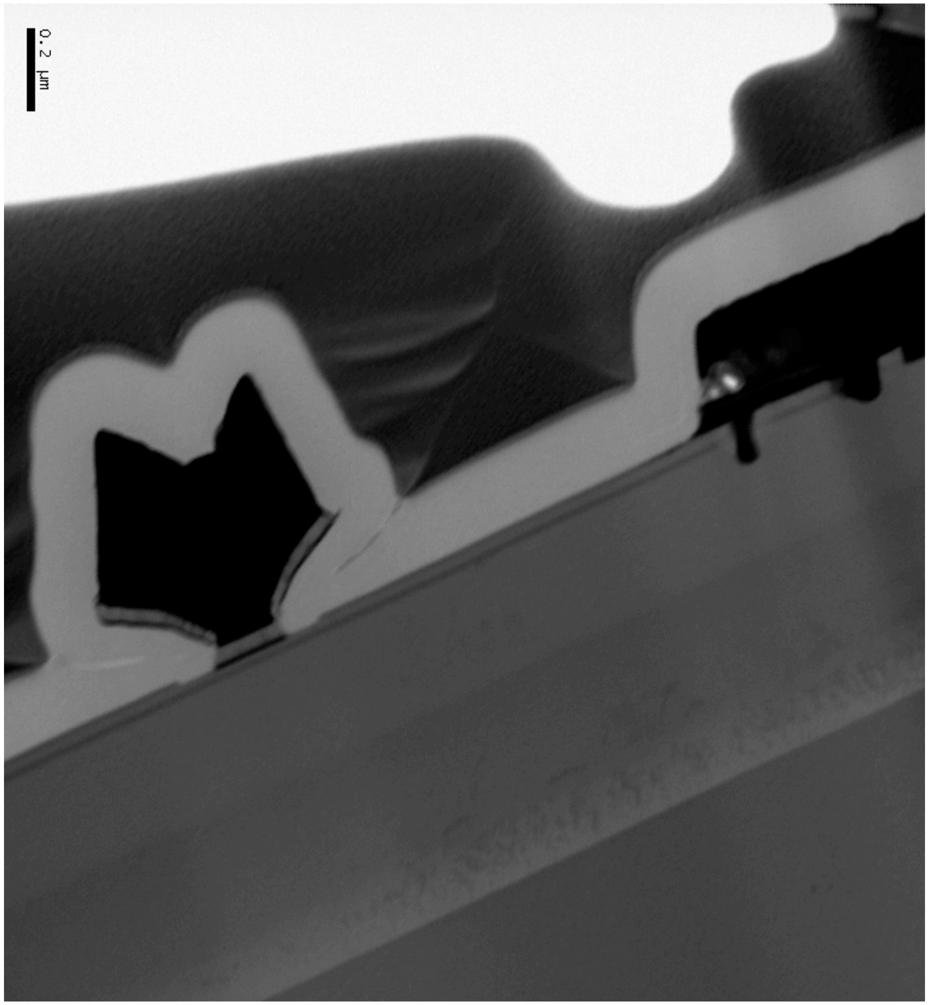
# Ohmic degradations found on the edge of metal contact pads



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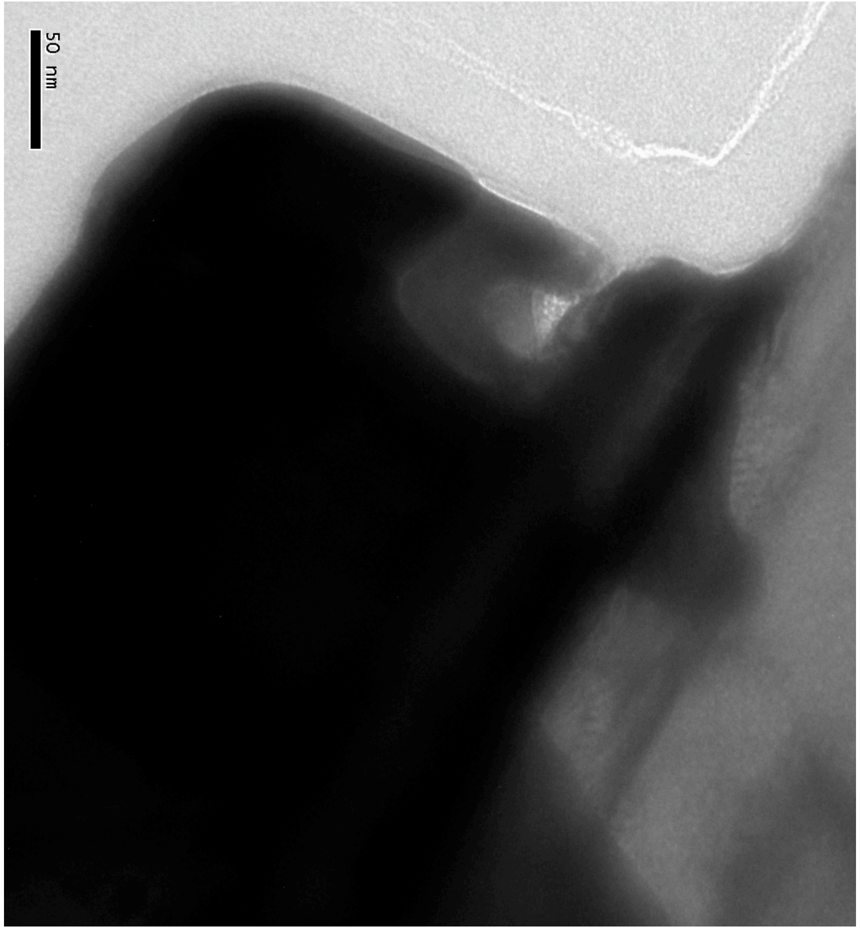


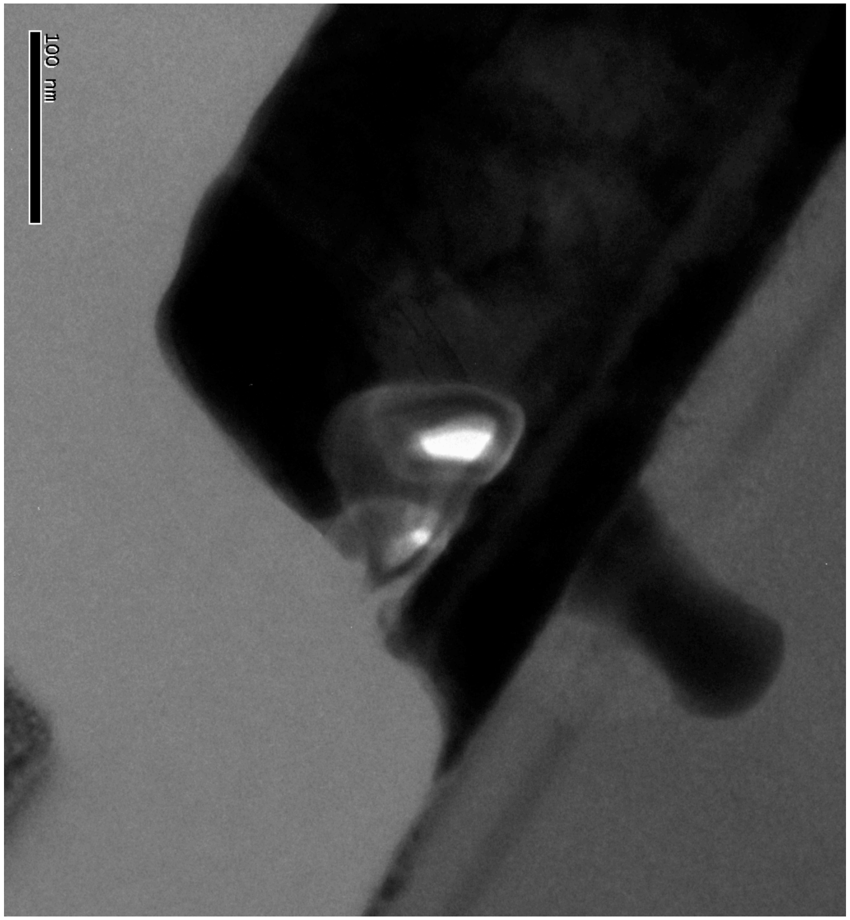


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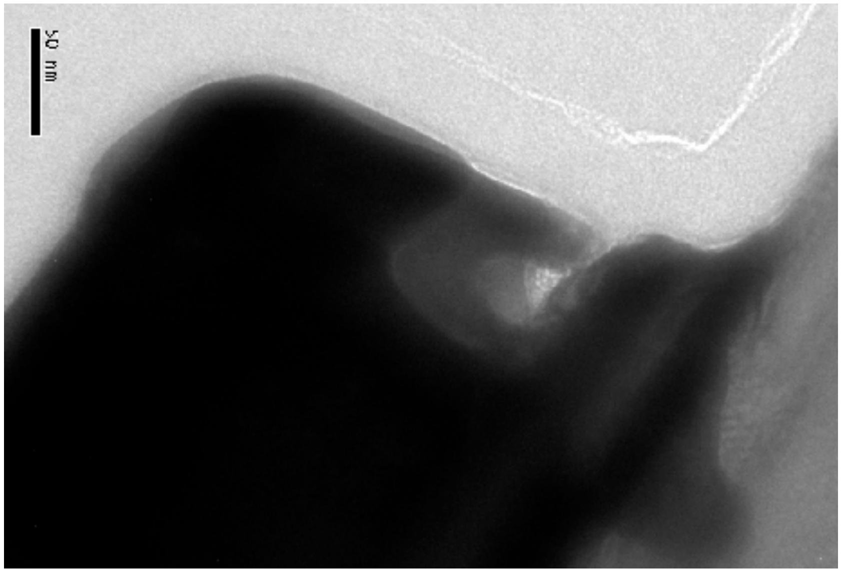
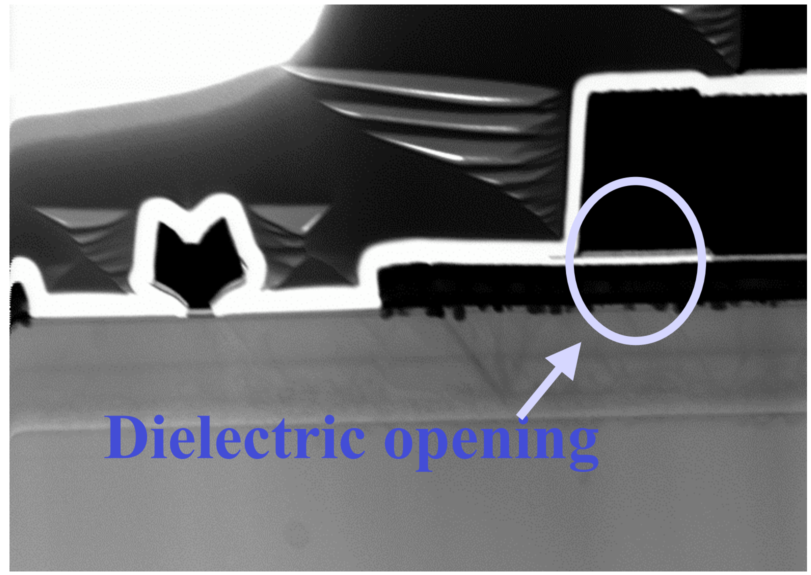
# Suggestions




**Ohmic metal thickness is roughly 250 nm. It is may be too thin to carry the current. [20 mA/(75 μm × 0.25 μm) = $1 \times 10^5$ A/cm$^2$ ] Is it possible to move the final metal pad closer to the edge of the ohmic metal? The dielectric opening window for the final metal has an overlap of 1 μm. This gap may enhance the electromigration problem.**

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# Summary and Conclusions

- What is the cause and can we eliminate or reduce the time for the burn-in process?
- Identified several problems, including gate sinking, dislocations, gate peeling. Gate sinking was intentionally introduced in the process to stabilize the gate characteristics. However, usually, the gm increases with the gate sinking (80-140 mV per nm gate sinking). This would not explain that gm decreased during the burn-in process. Therefore gate sinking was not the reason for degradation.
- We found some dislocations in stressed samples. However, we also found some dislocations in the unstressed sample, and could not be sure these were the causes for current degradation.
- TLM used to perform a stress study at UF to eliminate the gate sinking effect. We found the sheet resistance did not change-consistent with the TEM study for dislocation found in both stressed and unstressed samples. Thus the epi-layers was not the issue.
- Transfer resistance and contact transfer length did show significant degradation. These were consistent with our TEM study. We have found that Ohmic metal has been driven into the epi-layer around the edge of the contact and voids observed on both source and drain contact.
- We suggest that optimization of the Ohmic metal annealing conditions is needed and changes to the layout to eliminate electromigration are the main factors needed to reduce or eliminate the burn-in time for GaAs-based HEMTs
- We will now perform long term stress studies to see which mechanisms dominate the long-term stability

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